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Winstead Sechrest & Minick P.C.
P.O. Box 50784
1201 Main Street
Dallas, TX 75250-0784

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,100	CHOW ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121 (d) are required in this application because Figure 3 is informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 3, 4, 8, 9, 10, 11 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Mills (US Patent 5,991,303).

With regard to claims 1 and 8, Mills discloses a physical device 200 (HPNA control chip) that may be implemented on a chip (column 6, lines 13-14). The physical device 200 includes line driver I receiver circuit 250 (providing data path logic) (column 6, lines 16-21). In combination, auto-negotiation circuit 260 and management interface circuit 270 read on the applicant's consolidating the transmit data path logic to include transmit state machine (column 6, lines 16-21 and column 7, lines 1-5). Physical device interface 200 also includes a first

collision domain 210 a second collision domain 212 (two collision recovery means). Auto-negotiation circuit 260 provides seamless switching (minimal number of generic interface signals) between 100M and 10M domains (two data rate standards) without external switching circuitry (column 6, lines 60-65 and column 7, lines 61-65).

With regard to claims 2 and 9, auto-negotiation circuit 260 provides seamless switching (GO-signal) between 100M and 10M domains without external switching circuitry (column 7, lines 61-65).

With regard to claims 3 and 10, auto-negotiation circuit 260 provides seamless switching (new transmit signal) between 100M and 10M domains without external switching circuitry (column 7, lines 61-65).

With regard to claims 4 and 11, auto-negotiation circuit 260 provides seamless switching (done signal) between 100M and 10M domains without external switching circuitry (column 7, lines 61-65).

With regard to claim 15, Mills discloses a physical device 200 (HPNA control chip) that that may be implemented on a chip (column 6, lines 13-14). The physical device 200 includes line driver/receiver circuit 250 (physical layer) (column 6, lines 1621). Disclosed elements between front end multiplexer 240 and back end multiplexer 218 read on applicant's media access control (column 6, lines 16-21 and column 7, lines 1-5). Also, auto-negotiation circuit 260 and management interface circuit 270, in combination, read on the applicant's consolidating the transmit data path logic to include transmit state machine (column 6, lines 16-21 and column 7, lines 1-5). Physical device interface 200 includes MII circuit 214 (Mil) for communicating with a first collision domain 210 and Mll circuit 216 (Mll) for communicating

with a second collision domain 212 (two collision recovery means). Auto-negotiation circuit 260 provides seamless switching (minimal number of generic interface signals) between 100M and 10M (two data rate standards) domains without external switching circuitry (column 6, lines 60-65 and column 7, lines 61-65).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 6, 7, 12, 13, 14, 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mills (US Patent 5,991,303) in view of Lu et al hereinafter "Lu" (US Patent 6,839,345).

With regard to claims 5 and 12, Mills does not expressly disclose a transmit priority indicator from the transmit data. Lu discloses a deference algorithm module that implements distributed fair priority queuing DFPQ (priority) on HPNA 2.0 (column 4, lines 52-56).

A person of ordinary skill in the art to which the invention pertains would have been motivated to employ Lu in Mills to add DFPQ so as to provide a QOS guarantee at the physical layer (Lu, column 2, lines 17-19). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Mills and Lu (collectively "Mills--Lu") so as to obtain the invention as specified in claims 5 and 12.

With regard to claim 16, Mills discloses an auto-negotiation circuit 260 that provides seamless switching (GO-signal I new transmit signal I done signal) between 100M and 10M domains without external switching circuitry (column 7, lines 61-65).

Mills does not expressly disclose a transmit priority indicator from the transmit data. Lu discloses a deference algorithm module that implements distributed fair priority queuing DFPQ (priority) on HPNA 2.0 (column 4, lines 52-56).

A person of ordinary skill in the art to which the invention pertains to would have been motivated to employ Lu in Mills to add DFPQ so as to provide a QOS guarantee at the physical layer (Lu, column 2, lines 17-19). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Mills and Lu (collectively "Mills-Lu") so as to obtain the invention as specified in claim 16.

With regard to claims 6, 13 and 17, Mills does not expressly disclose that the at least two separate collision recovery means further comprises a BEB collision recovery means. Lu discloses a deference algorithm module that implements BEB (BEB) on HPNA 1.0 (column 4, lines 52-56).

A person of ordinary skill in the art to which the invention pertains to would have been motivated to employ Lu in Mills to employ binary exponential backoff algorithm to defer its transmission when media is busy (Lu, column 2, lines 12-17). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Mills and Lu (collectively "Mills-Lu") so as to obtain the invention as specified in claims 6, 13, and 17.

With regard to claims 7, 14 and 18, Lu discloses a deference algorithm module that implements DFPQ (DFPQ) on HPNA 2.0 (column 4, lines 52-56). The motivation can be found in Lu, by adding DFPQ method, it would provide a QoS guarantee at the physical (see Lu col. 2, line 17-19), which the same motivation as recited for claims 5 and 12.

Response to Arguments

6. Applicant's arguments filed 5/23/2005 have been fully considered but they are not persuasive.

Regarding claims 1-4,8-11 and 15, the applicant argued that, "...Mills does not disclose "providing transmit data path logic to receive transmit data packets within the HPNA control chip"..." in page 3, paragraph 4.

In response to applicant's argument, the examiner respectfully disagrees with the above argument.

Mills discloses providing transmit data path logic (see FIG. 5, line driver/receiver 250) to receive transmit data packets (see col. 6, line 10-12; packets) within the HPNA control chip (see col. 6, line 13-14, 16-21; a chip that couples to twist pair wire, that is, T. Note that twist pair wire is well known in the art is used for home/residential wiring (see cited text book, Stallings, chapter 4.1). Moreover, Mills's chip utilizes Ethernet 802.xx standard with twist pair connection for home/residential wired networking, which is analogous to applicant's home phoneline networking alliance (HPNA) control chip since both claimed invention and Mills have identical functionality. Thus, Mills clearly anticipates the applicant's argued limitations.

Regarding claims 1-4,8-11 and 15, the applicant argued that, "...Mills does not disclose "consolidating the transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of the HPNA control chip through a minimal number of generic interface signals"... applicant were unable to identify the phrase "state machine" or any variation thereof in Mills... " in page 3, paragraph 4; page 4, paragraph 1; page 6, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with the above argument.

Mills discloses consolidating the transmit data path logic (see FIG. 5, consolidating/combining the processes/logic of line driver/receiver 250) to include a transmit state machine (see FIG. 5, a combined system of auto-negotiation circuitry 260 and management interface circuit 270; see col. 6, line 16-21; col. 7, line 1-5) that handles interfacing the transmit data path logic (see FIG. 5, a combined system 260 and 270 handles the interfacing the line/driver 250; see col. 6, line 16-21) to at least two separate collision recovery logic means of the HPNA control chip (see FIG. 5, first collision domain 210 and second collision domain 212) through a minimal number of generic interface signals (see FIG. 5, via 10 Mbps interface signal/domain (utilizing **IEEE** standard/generic 10 base T physical device circuitry 220) and/or 100 Mbps interface signal/domain (utilizing **IEEE** standard/generic 100 base T physical device circuitry 230); see col. 6, line 60-65; see col. 7, line 61-65).

As recited in the previous office action, the examiner asserts the "state machine" as "a combined/combination of auto-generation circuit 260 and management interface circuit 270"

since both "state machine" and the combined system of 260 and 270 have identical functionality.

Regarding claim 8, the applicant argued that, "...Mills does not disclose "at least two separate collision recovery logic in the HPNA control chip according to at least two data rate standards"..." in page 4, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with the above argument.

As recited in previous office action page 3, Mills discloses at least two separate collision recovery logic in the HPNA control chip (see FIG. 5, first collision domain 210 and second collision domain 212) according to at least two data rate standards (see FIG. 5, 10 Mbps interface signal/domain (utilizing **IEEE** standard/generic 10 base T physical device circuitry 220) and 100 Mbps interface signal/domain (utilizing **IEEE** standard/generic 100 base T physical device circuitry 230); see col. 6, line 60-65; see col. 7, line 61-65). It is well known in the art that IEEE 802 standard/generic defines 10 Mbps and 100 Mbps as standard rates.

Regarding claim 15, the applicant argued that, "...Mills does not disclose "a physical layer (PHY)"..." in page 5, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. As recited in previous office action, examiner asserts Mills's line driver/receiver circuit 250 is a physical layer; see col. 6, line 16-21. Mills also discloses the MAC and IEEE 802 standard (see col. 6, line 6-26). Also, in accordance with IEEE 803 standard, as one skill in the ordinary art would clearly recognize, that the physical layer must

be present, otherwise, one will not be able to transmit/receiver data at all per the following prior arts:

a) Stalling, textbook, for IEEE 802 protocol stack, chapter 13.2

b) McLaughlin (US006269104B1), FIG. 1, see col. 2, line 65 to col. 3, line 50

c) Mallory (US 20020057717A1), FIG. 4A

Thus, Mills clearly anticipates the argued limitation.

Regarding claim 15, the applicant argued that, "...Mills does not disclose, "a media access controller (MAC) coupled between the MII and the physical layer (PHY)"...there is no language that discloses media access controller" in page 5, paragraph 3..

In response to applicant's argument, the examiner respectfully disagrees with the above argument. As recited in previous office action, examiner asserts Mills's medium access control (see FIG. 5, multiplexers 240 and 218 and MAC; see col. 6, line 9-12; also see FIG. 10, MAC 712 and 714; see col. 11, line 52-65) coupled between MII (see FIG. 5, MII 214 and 216) and the physical layer (see FIG. 5, line driver/receiver circuit 250). Mills also discloses IEEE 802 standard (see col. 6, line 6-26). Also, the arrangement (i.e. PHY-MAC-Media independent Interface (MII)) in well known in the art and IEEE 802 standard, as accordance with the following prior arts:

a) McLaughlin (US006269104B1), FIG. 1, see col. 2, line 65 to col. 3, line 50

b) Mallory (US 20020057717A1), FIG. 4A

c) Eson (US 20030101459A1), FIG. 3, paragraph 61

Thus, Mills clearly anticipates the argued limitation.

Regarding claim 15, the applicant argued that, "...Mills does not disclose, "the MAC further comprising at least two collision recovery means for providing collision recovery according to at least two data rate standards "..." in page 6, paragraph 32; page 7, paragraph 1.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. Mills discloses MAC further comprising at least two collision recovery means (see FIG. 5, first collision domain 210 and second collision domain 212) for providing collision recovery according to at least two data rate standards (see FIG. 5, 10 Mbps interface signal/domain (utilizing **IEEE** standard/generic 10 base T physical device circuitry 220) and 100 Mbps interface signal/domain (utilizing **IEEE** standard/generic 100 base T physical device circuitry 230); see col. 6, line 60-65; see col. 7, line 61-65). It is well known in the art that IEEE 802 standard/generic defines 10 Mbps and 100 Mbps as standard rates.

Regarding claim 15, the applicant argued that, "...Mills does not discloses "wherein the minimal number of interface signals further comprises "a GO signal", "a new transmit signal" or "a transmit done" signal from each separate collision recover logic means "..." in page 7, paragraph 3; page 8, paragraph 2-3; page 12, paragraph 2-3.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. Mills discloses "a GO signal", "a new transmit signal" or "a transmit done" signal from each separate collision recover logic means (see col. 7, line 60-65; 10-35; first and second control signals triggering (i.e. when to initiate, start/go, stop) the auto generation process between the interface signals, in order to avoid collision). When performing auto generating, the process must determines and arbitrates when to initiates, start/go, or stop by

means of a control signal in order to control and recover the collision. Moreover, Mills also discloses that collision detection in accordance is in accordance with IEEE 802.3 standard, that is, Medium Access Control implementing CSMA/CD, Ethernet, Token Ring, or the like, which utilizes the signals/tokens to avoid collision.

Regarding claim 5 and 12, the applicant argued that, "...examiner's motivation is insufficient to support a prima facie case of obviousness...examiner motivation "to provide a QOS guarantee at the physical layer" does not address as why one of ordinary skill in the art would modify Mills...examiner is merely relying upon his own subjective opinion "..." in page 9, paragraph 3 and page 10, paragraph 1.

In response to applicant's argument that there is <u>insufficient</u> motivation to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Note that the applicant argues that "there is insufficient motivation", and the applicant also recites the motivation "to provide a QOS guarantee at the physical layer" as described by Lu, in col. 2, lines 17-19, thereby the applicant is admitting that **<u>there is</u> a motivation**.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. Lu clearly teaches how one could implement DFPQ method in accordance IEEE 802.3, for prioritization. Therefore, it would have been obvious to one having ordinary

skill in the art at the time the invention was made to provide priority indicator, as taught by Lu in the system of Mills, so that it would provide a QoS guarantee at the physical layer; see Lu col. 2, line 17-19. In addition, it should be clear to one skill in the art that why one would need a priority indicator, evidently because one need to provide quality of service guarantee transmission. Thus, it is clear that cited motivation is neither the examiner's subjective opinion nor insufficient.

Regarding claim 6,13, and 17, the applicant argued that, "...examiner's motivation is insufficient to support a prima facie case of obviousness...examiner motivation does not address as why one of ordinary skill in the art with the primary reference (Mills) in front of him would modify to have separate collision recovery logic means a BEB collision recovery means...examiner is merely relying upon his own subjective opinion "..." in page 10, paragraph 2-3; page 11, paragraph 1; page 13, paragraph 3.

In response to applicant's argument that there is <u>insufficient</u> motivation to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Note that the applicant argues that "there is insufficient motivation", and the applicant also recites the motivation "to defer its transmission when media is busy" as described by Lu, in col. 2, lines 12-17, thereby the applicant is admitting that **<u>there is</u> a motivation**.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. Lu clearly teaches how one could implement Binary Exponential Backoff (BEB) method in accordance IEEE 802.3, to avoid collision. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide priority indicator, as taught by Lu in the system of Mills, so that it would provide a BEB to defer its transmission when media is busy; see Lu col. 2, line 12-17. In addition, it should be clear to one skill in the art that why one would need to employ a BEB, evidently because one needs to defer its transmission when media is busy, so that one can avoid collision. Thus, it is clear that cited motivation is neither the examiner's subjective opinion nor insufficient.

Regarding claim 7,14, and 18, the applicant argued that, "...examiner does not provide any motivation for modifying Mills with Lu "..." in page 11, paragraph 2; page 13, paragraph 4.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation can be found in Lu, by adding DFPQ method, it would provide a QoS guarantee at the physical (see Lu col. 2, line 17-19), which the same motivation as recited for claims 5 and 12.

Regarding claim 5 and 12, the applicant argued that, "...there is no language in the cited passages that a minimal number of interface signals includes "a transmit priority indicator from the transmit data "..." in page 11, paragraph 3; page 12, paragraph 1; page 13, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. Mills discloses a minimal number of interface signals from the transmit data as described above rejection and response. Lu discloses distributed fair priority queue (DFPQ) method and prioritizing in MAC architecture (see col. 5, line 30-36, 50-60; see col. 8, line 10-14). Note that it is well known in the art that **DFPQ** method utilizes a transmit priority indicator "PRI" from the transmit data in accordance with IEEE 802.3 standard, as clearly recited by Mollory (US 20020057717A0), FIG. 7 and 8 with PRI 620 field, which can be defined from 0-7, see paragraphs 173, 174, 498, where transmit priority indicator PRI defines the DFPQ. Thus, it is clear that when one is implementing DFPQ method, one must use PRI as a transmit priority indicator from the transmit data. Thus, Lu clearly anticipates the argued limitation.

The applicant argued that, "...examiner has not presented a reasonable expectation of success when combining Mills with Lu....Examiner must provide...how a multi-communication rate switching physical device for recovering bits from a wire connection can be combined with a system that manages data flow rate over an open system interconnection type network..." in page 14, paragraph 2; page 15, paragraph 1.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are

based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that examiner has not presented a reasonable expectation of success, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument, the examiner respectfully disagrees with the above argument. As recited in the previous rejections and in accordance with the above responses, there are motivations to combine Mills with Lu, and by implementing/employing DFPQ method, BEB method, and DFPQ with priority indicator taught by Lu to Mills system, one can simply achieve the applicant claimed invention.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that the reference(s) as set forth in the 102 and 103 rejections are proper.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

INM
9/14/05